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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,603	12/28/2001	Robert M. English	112056-0036	3815

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/035,603	ENGLISH ET AL.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,17,18 and 24-27* is/are rejected.

7)☒ Claim(s) *11-16 and 19-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28, 3/12, 3/25*, 6/3/2002, 3/28/03
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending and are hereby presented for examination, in response to the present Application filed 12/28/2001.

Specification

2. The abstract of the disclosure is objected to because of legal phraseology. On line 3, "comprises" should be changed to "includes". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10, 17-19, 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Han et al. (US 6158017).

Regarding Claims 1, 2, 3, 26, 27, Han discloses (FIG. 2) a structure of a disk array for correcting storage device failures arranged in a combination of first and secondary parity groups corresponding to diagonal and horizontal parity groups together with parity blocks (DH2), as shown in FIG. 4, comprising:

A storage disk array defined as a matrix of (N-1)* (N+1) having a plurality of concatenated sub-arrays (N+1 disks) each logically divided into N-1 data blocks of a row being defined as a horizontal parity group and as a diagonal

parity group, defining the data blocks of the last disk as the horizontal parity blocks, and defining the data blocks existing in the (N-1) row of the matrix as the diagonal parity blocks. The contents of each of the horizontal and diagonal parity groups are logically (XOR) to obtain the parity value stored into the parity block of the corresponding horizontal or diagonal parity group, and further analyzing the diagonal parity group and the horizontal parity group to restore error data block, where the analyzing step is repeated to completely rebuilt the data contents of the failed disks. The secondary parity values, such as the diagonal parity group values, are computed across the concatenation of the sub-arrays, according to diagonal parity blocks and groups (Definition 6) (Summary of the Invention, Col. 3, lines 20-40). Also, refer to (FIGS. 4 and 8 to 10), for a structure of the DH2 parity arrangement (Definition 4), horizontal parity blocks and groups (Definition 5), diagonal parity blocks and groups (Definition 6).

Regarding Claims 10, 24, 25, Han discloses the pertinent limitations as applied to Claim 1, above and in addition he discloses means for computing the diagonal parity for the single diagonal parity group across the concatenated sub-arrays, according to (Definition 6) for defining the Diagonal Parity Groups and Blocks in DH2 Parity Arrangement. "The data blocks, existing in each rightwardly and upwardly closed looped diagonal line, are defined as an error correction group of diagonal parities". Also, "FIG. 10 depicts the arrangement of the parities and data in the form of a matrix in the case of N=7 in the DH2 parity arrangement. Reference numerals H0 to H4 represent the horizontal parity blocks of the horizontal parity group Nos. 0 to 5, and D0 to D6 represent the

diagonal parity blocks of the diagonal parity group Nos. 0 to 6. Each of the data blocks is identified by i and j, where i represents the horizontal parity groups and j the diagonal parity groups.

Correcting the storage device failure within the array using the row parity storage device associated with each sub-array and the global diagonal parity storage device associated with the storage array, including the step of "analyzing a diagonal parity group including an error data block of the two failed disks to restore the error data block and then, the horizontal parity group including the restored error data block to restore another error data block, wherein the last analyzing step is repeated to completely rebuild the data contents of the two failed disks" (See Abstract).

Regarding Claims 4, 5, Han discloses (controller 4, FIG. 2) for performing an encoding and decoding algorithm of the DH2 parity arrangement, FIG. 2. The parity storage algorithm provides a method for obtaining the parity values of the data blocks of the parity groups by XOR'ing, FIG. 15. The disk array of (N-1)*(N+1) is controlled by the controller 4 (FIG. 2) to store the horizontal and diagonal parities respectively, steps (210 and 220). In step 210, the controller 4 calculates upon the horizontal parities of the horizontal parity group Nos. 0 to (N-3) to encode the horizontal parity blocks with the corresponding horizontal parities. In step 220, the controller calculates the diagonal parities of the diagonal parity group Nos. 0 to (N-1) to encode the diagonal parity blocks with the corresponding diagonal parities.

Regarding Claim 6, Han discloses EVENODD parity encoding, illustrating a map of parity blocks (when disk number N=7) to be accessed to update diagonal S blocks in an EVENODD arrangement, FIG. 25.

Regarding Claims 7, 8, 17, 18, Han discloses a plurality of concatenated sub-arrays (N+1 disks) each logically divided into N-1 data blocks, FIGS. 2 and 4, wherein each sub-array (DISK) is organized as a distributed parity disk array (FIGS. 4 and 8 to 10).

Regarding Claim 9, Han discloses storage devices, which is magnetic disk device.

Allowable Subject Matter

4. Claims 11-16 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior arts of record taken alone or in combination fail to teach, anticipate, suggest or render obvious the claimed invention included in the claims for the reasons described below:

Claims 11 and 19 include the method steps of determining whether the storage device failure is to a single storage device in a sub-array; if the storage device failure is to a single storage device in the sub-array, reconstructing the failed storage device using local row parity associated with the sub-array; and if the storage device failure is not to a single storage device in the sub-array,

reconstructing the failed global diagonal parity storage device using all data and row parity storage devices of all sub-arrays of the array.

Claims 12-16 and 20-23 are objected over the prior arts of record, becuase they are directly or indirectly depended upon claims 11 and 19.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Raphaeli et al. (US 6654926) discloses a method of generating a soft decision error correcting code, including the steps of initializing a horizontal parity symbol, initializing a diagonal parity symbol, receiving a block of data comprising a plurality of symbols, and for each symbol, XORing the symbol with the horizontal parity symbol, XORing the symbol with the diagonal parity symbol, and calculating an `S` bit from the data block.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 19 August 2004
Office Action: Non-Final Rejection

By: _____

James C Kerveros
Examiner
Art Unit 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100